In the Claims:

Please amend the claims 1, 3-11, 17-31, 34, 35, 41, 43, 45-48, 51, 52, 55-58, 61, 62, 66, 67, 72 and 73, and please cancel claims 2, 12-16, 32, 33, 36-40, 42, 44, 49, 50, 53, 54, 59, 60, 63-65 and 68-71, as indicated below.

1. (Currently amended) A computer readable storage medium storing program instructions executable by a processor of a multithreaded system to implement a mutual exclusion mechanism comprising:

a biasable lock that is concurrently accessible to a plurality of threads on the multithreaded system and is biased to at most one of the plurality of threads at a given time; ~~and~~

acquisition and release sequences that, when executed by a bias-holding thread on the processor, ~~to which~~ wherein the biasable lock is biased to the bias-holding thread ~~has been directed~~, are free of atomic read-modify-write operations and of memory barrier operations executable to constrain the processor from performing at least one type of instruction reordering; and

wherein the processor supports out-of-order instruction execution.

2. (Canceled)

3. (Currently amended) The ~~mutual exclusion mechanism~~ computer readable storage medium of claim 1,

wherein the acquisition and release sequences include only read and write operations when executed by the bias-holding thread ~~to which bias has been directed~~.

4. (Currently amended) The ~~mutual exclusion mechanism~~ computer readable storage medium of claim 1,

wherein the biasable lock is initially unbiased.

5. (Currently amended) The ~~mutual exclusion mechanism~~ computer readable storage medium of claim 1,

wherein the biasable lock is biased on creation.

6. (Currently amended) The ~~mutual exclusion mechanism~~ computer readable storage medium of claim 1,

wherein the biasable lock is biased on acquisition.

7. (Currently amended) The ~~mutual exclusion mechanism~~ computer readable storage medium of claim 1,

wherein the bias-holding ~~is directed to a~~ thread is not the ~~other than a~~ creating thread.

8. (Currently amended) The ~~mutual exclusion mechanism~~ computer readable storage medium of claim 1,

wherein execution of the acquisition sequence by the bias-holding thread employs a programming construct that precludes reordering of a particular read before a particular write.

9. (Currently amended) ~~mutual exclusion mechanism~~ computer readable storage medium of claim 8,

wherein the precluded reordering includes reordering by a compiler.

10. (Currently amended) The ~~mutual exclusion mechanism~~ computer readable storage medium of claim 8,

wherein the precluded reordering includes reordering ~~upon execution~~ by [[a]] the processor.

11. (Currently amended) The ~~mutual exclusion mechanism~~ computer readable storage medium of claim 8,

wherein the programming construct employs collocation of the target of the particular read and the target of the particular write.

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Cancelled)

17. (Currently amended) The ~~mutual exclusion mechanism~~ computer readable storage medium of claim 8,

wherein the particular read loads lock status; and

wherein the particular write stores a quick lock indication.

18. (Currently amended) The ~~mutual exclusion mechanism~~ computer readable storage medium of claim 8,

wherein the preclusion is based, at least in part, on characteristics of an implementation of a memory model implemented by the processor.

19. (Currently amended) The ~~mutual exclusion mechanism~~ computer readable storage medium of claim [[8]] 1,

~~embodied in code compiled for execution on a~~ the processor ~~that~~ implements a total store order (TSO) memory model,

wherein the acquisition by the bias-holding lock ~~programming construct~~ includes ~~use of~~ a store operation followed in program order by a load operation, the store and load operations having collocated targets that encode a quick lock indication and lock status, respectively.

20. (Currently amended) The ~~mutual exclusion mechanism~~ computer readable storage medium of claim 1,

wherein the biasable lock includes an MCS lock augmented to provide fast path acquisition and release sequences for the bias-holding thread ~~to which bias has been directed~~.

21. (Currently amended) The ~~mutual exclusion mechanism~~ computer readable storage medium of claim 1,

wherein the biasable lock includes an TAT AS lock augmented to provide fast path acquisition and release sequences for the bias-holding thread ~~to which bias has been directed~~.

22. (Currently amended) The ~~mutual exclusion mechanism~~ computer readable storage medium of claim 1,

wherein the biasable lock includes a lock provided by a POSIX pthreads mutex library, augmented to provide fast path acquisition and release sequences for the bias-holding thread ~~to which bias has been directed~~.

23. (Currently amended) The ~~mutual exclusion mechanism~~ computer readable storage medium of claim 1,

wherein the biasable lock includes a monitor provided by a Java virtual machine implementation, the monitor augmented to provide fast path acquisition and release sequences for the bias-holding thread ~~to which bias has been directed~~.

24. (Currently amended) The ~~mutual exclusion mechanism~~ computer readable storage medium of claim 1,

wherein the biasable lock is rebiasable to another thread during course of a computation that employs the lock.

25. (Currently amended) The ~~mutual exclusion mechanism~~ computer readable storage medium of claim 1,

wherein bias of the lock to the bias-holding thread is revocable and revocation of bias by, or on behalf of, a contending thread, is mediated, at least in part, using a signal handler.

26. (Currently amended) The ~~mutual exclusion mechanism~~ computer readable storage medium of claim 1,

wherein bias of the lock to the bias-holding thread is revocable and revocation of bias by, or on behalf of, a contending thread, is mediated, at least in part, using a cross-call.

27. (Currently amended) The ~~mutual exclusion mechanism~~ computer readable storage medium of claim 1,

wherein bias of the lock to the bias-holding thread is revocable and revocation of bias by, or on behalf of, a contending thread, is handled, at least in part, at a garbage collection safe point.

28. (Currently amended) The ~~mutual exclusion mechanism~~ computer readable storage medium of claim 24, ~~further comprising~~ wherein the program instructions are further executable to implement:

~~means for~~ detecting a current level of contention;

revoking the bias of the biasable lock in response to detecting a given level of contention; and

a rebiasing sequence ~~that~~ executable by the processor to rebias[[es]] the lock to the thread in response to detecting~~ion of an absence~~ a lower level of contention.

29. (Currently amended) The ~~mutual exclusion mechanism~~ computer readable storage medium of claim 28,

wherein the detecting a current level of contention detection ~~means accesses~~ comprises accessing a request queue to identify the ~~absence~~ level of contention.

30. (Currently amended) The ~~mutual exclusion mechanism~~ computer readable storage medium of claim [[1]] 28,

wherein the detecting a current level of contention detection ~~means employs~~ comprises employing an attempt counter to identify the ~~absence~~ level of contention.

31. (Currently amended) A computer readable storage medium storing program instructions executable by a processor of a multithreaded system to implement a biasable lock ~~that~~ wherein:

the bias able lock is concurrently accessible to a plurality of threads on the multithreaded system and is biased to at most one of the plurality of threads at a given time;

the biasable lock provides at least two acquisition sequences including [[,]] a fast path acquisition sequence for a bias-holding thread to which the biasable lock has been biased and a second acquisition sequence, the fast path acquisition sequence optimized ~~with respect~~ relative to the second acquisition sequence;

wherein the fast path acquisition sequence is free of atomic read-modify-write operations and of explicit memory barrier operations executable to constrain the processor from performing at least one type of instruction reordering; and

wherein the processor supports out-of-order instruction execution.

32. (Cancelled)

33. (Cancelled)

34. (Currently amended) The ~~biasable lock~~ computer readable storage medium of claim 31,

wherein the second acquisition sequence implements one of an MCS lock, a TAT AS lock, a lock consistent with that provided by a POSIX pthread Mutex library and a Java monitor.

35. (Currently amended) The ~~biasable lock~~ computer readable storage medium of claim 31,

wherein the biasable lock is ~~further~~ rebiasable.

36. (Currently amended) A computer-implemented method ~~of providing an efficient locking mechanism in program code~~, the method comprising:

instantiating a biasable lock that is concurrently accessible to a plurality of threads on the multithreaded system and is biased to at most one of the plurality of threads at a given time; and

for [[a]] the thread to which bias has been directed, releasing and acquiring the biasable lock using fast path instruction sequences that are free of atomic read-modify-write operations and of explicit memory barrier operations

executable to constrain the processor from performing at least one type of instruction reordering.

37. (Original) The method of claim 36, further comprising:
directing the bias to the thread coincident with a first acquisition of the biasable lock.

38. (Original) The method of claim 36, further comprising:
directing the bias to the thread coincident with the instantiation.

39. (Original) The method of claim 36, further comprising:
directing the bias to the thread coincident with creation of an object.

40. (Original) The method of claim 36,
wherein directing of bias to the thread is performed by another thread.

41. (Currently amended) The method of claim 36, further comprising:
for a thread other than the thread to which bias has been directed, acquiring the lock using an instruction sequence that unbiases the lock, if ~~then~~ it is biased.

42. (Currently amended) The method of claim 36, further comprising:
rebiasing the biasable lock to another thread.

43. (Currently amended) The method of claim 36, further comprising: executing the program code as a multi-threaded software application [[,]] configured to utilize the biasable lock to allow~~ing a single~~ the bias-holding thread of the ~~executing program code~~ multi-threaded software application to repeatedly acquire and release the biasable lock, at least in part by executing one or more of the fast path instruction sequences ~~with extremely low overhead~~.

44. (Currently amended) The method of claim 43, further comprising: after rebiasing to another thread, allowing the another thread to repeatedly acquire and release the lock with extremely low overhead.

45. (Currently amended) The method of claim 36, ~~further comprising:~~ wherein the method is performed as part of executing ~~the~~ program code in a single-threaded execution environment,

wherein the program code is compiled with the biasable lock for execution on both the single-threaded execution environment and on a multi-threaded execution environment, and

wherein the biasable lock allows the program code to run in the single-threaded execution environment without significant lock-related overhead.

46. (Currently amended) A computer readable storage medium storing program instructions executable by a processor of a multithreaded system to implement:

a biasable software lock that that is concurrently accessible to a plurality of threads on the multithreaded system and is biased to at most one of the plurality of threads at a given time and maintains both a lock state and bias state, whereby acquisition of the lock by a thread to which bias has been directed is more efficient than acquisition of the lock by another thread and does not include any atomic read-modify-write operations or memory barrier operations executable to constrain the processor from performing at least one type of instruction reordering; and

wherein the processor supports out-of-order execution.

47. (Currently amended) The ~~lock~~ computer readable storage medium of claim 46,

wherein the lock is rebiasable to another thread during course of a computation that employs the lock.

48. (Currently amended) The ~~lock~~ computer readable storage medium of claim 46, including acquisition and release sequences that, when executed by the thread to which bias has been directed, include only read and write operations ~~are free of atomic read-modify-write operations~~.

49. (Cancelled)

50. (Cancelled)

51. (Currently amended) The ~~lock~~ computer readable storage medium of claim 48,

wherein the acquisition sequence employs a programming construct that precludes reordering of a particular read before a particular write.

52. (Currently amended) A computer readable storage medium storing program instructions executable by one or more processors of a multithreaded system to implement a program product including a mutual exclusion mechanism embodied therein, the ~~computer~~ program product ~~embodied in a computer readable medium and~~ comprising:

a data structure instantiable in memory of a processor to implement a lock that includes a bias attribute, wherein the lock is concurrently accessible to a plurality of threads on the multithreaded system and is biased to at most one of the plurality of threads at a given time; ~~and~~

a lock acquisition sequence of operations executable by the processor, the lock acquisition sequence having a fast path for a thread to which bias has been directed and a second path, the fast path optimized ~~with respect~~ relative to the second path;

wherein the fast path acquisition sequence is free of atomic read-modify-write operations and of explicit memory barrier operations executable to constrain the processor from performing at least one type of instruction reordering; and

wherein the processor supports out-of-order instruction execution.

53. (Cancelled)

54. (Cancelled)

55. (Currently amended) The computer readable storage medium ~~program product~~ of claim 52, further comprising:

a lock release sequence of operations executable by the processor, the lock release sequence having a fast path for the thread to which bias has been directed and a second path, the fast path optimized ~~with respect~~ relative to the second path.

56. (Currently amended) The computer readable storage medium ~~program product~~ of claim 52,

wherein the acquisition sequence employs a programming construct that precludes reordering of a particular read before a particular write.

57. (Currently amended) The computer readable storage medium ~~program product~~ of claim 52,

wherein the lock is rebiasable to another thread during course of a computation that employs the lock.

58. (Currently amended) A computer implemented ~~software~~ method comprising:

a computer processor that supports out-of-order instruction execution performing:

biasing a lock to a first thread of execution, wherein the biasable lock is concurrently accessible to a plurality of threads and is biased to at most one of the plurality of threads at a given time; and

subsequently acquiring the lock for, or by, the first thread with computational overhead ~~substantially~~ less than for a second thread to which the lock is not currently biased, wherein said acquiring is performed free of atomic read-modify-write operations and of explicit memory barrier operations executable to constrain the processor from performing at least one type of instruction reordering.

59. (Cancelled)

60. (Cancelled)

61. (Currently amended) The computer implemented method of claim 58, further comprising:

rebiasing the lock to a third thread of execution.

62. (Currently amended) A computer system, comprising:

a processor coupled to one or more other processors and configured to perform out-of-order instruction execution;

a memory coupled to the processor, the memory storing program ~~product encoding~~ instructions executable by the processor ~~that~~ to implement:

a biasable lock that is concurrently accessible to a plurality of threads on the multithreaded system and is biased to at most one of the plurality of threads at a given time;

acquisition and release sequences that, when executed by a bias-holding thread on the processor, wherein the biasable lock is biased to the bias-holding thread, do not comprise executing atomic read-modify-write operations or explicit memory barrier operations executable to constrain the processor from performing at least one type of instruction reordering.

63. (Cancelled)

64. (Cancelled)

65. (Cancelled)

66. (Currently amended) The computer system ~~program product~~ of claim 62, further comprising:

a rebiasing sequence, executable by the processor to bias the biasable lock to another thread on the system instead of to the bias-holding thread.

67. (Currently amended) The computer system ~~program product~~ of claim 62, wherein the memory is implemented as ~~embodied in~~ at least one computer readable storage medium selected from the set of a disk, tape or other magnetic, optical, or electronic storage medium ~~and a network, wireline, wireless or other communications medium~~.

68. (Cancelled)

69. (Cancelled)

70. (Cancelled)

71. (Cancelled)

72. (Currently amended) A computer implemented method of making a single computer program product suitable for efficient execution as both a single-threaded computation and a multi-threaded computation on one or more processors capable of out-of-order execution, the method comprising:

structuring a computation as a ~~potentially~~ multithread computation;

mediating at least some sources of contention in the multithreaded computation using a bias[[ ]]able locking mechanism, wherein the biasable locking mechanism is concurrently accessible to a plurality of threads on the one or more processors and is biased to at most one of the plurality of threads at a given time;

wherein the said mediating includes providing at least two acquisition sequences including a fast path acquisition sequence for a bias-holding thread to which the biasable lock has been biased and a second acquisition sequence, the fast path acquisition sequence being optimized relative to the second acquisition sequence;

~~and~~ introducing the instances of the biasable locking mechanism into program code;

compiling the program code; and

encoding the compiled program code, including the instances of the biasable locking mechanism, in a computer program product.

73. (Currently amended) The method of claim 72,

wherein the encoding includes transferring the compiled program code onto at least one computer readable storage medium selected from the set of a disk, tape or other magnetic, optical, or electronic storage medium ~~and a network, wireline, wireless or other communications medium~~.